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Electronic transport in a two-dimensional superlattice engineered via self-assembled nanostructures

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Nanoscience offers a unique opportunity to design modern materials from the bottom up via low-cost, solution processed assembly of nanoscale building blocks. These systems promise electronic band structure engineering using not only the nanoscale structural modulation, but also the mesoscale spatial patterning, although experimental realization of the latter has been challenging. Here, we design and fabricate a new type of artificial solid by stacking graphene on a self-assembled, nearly periodic array of nanospheres, and experimentally observe superlattice miniband effects. We find conductance dips at commensurate fillings of charge carriers per superlattice unit cell, which are key features of minibands that are induced by the quasi-periodic deformation of the graphene lattice. These dips become stronger when the lattice strain is larger. Using a tight-binding model, we simulate the effect of lattice deformation as a parameter affecting the inter-atomic hopping integral, and confirm the superlattice transport behavior. This 2D material-nanoparticle heterostructure enables facile band structure engineering via self-assembly, promising for large-area electronics and optoelectronics applications.

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INTRODUCTION

Band structure engineering is key to realizing next-generation electronic and optoelectronic devices. One promising approach toward this goal is superlattice modulation, i.e., engineering long-range periodic patterns to artificially tailor the electronic band structure. This artificial lattice can have a periodicity in the range of 1–50 nm, which is shorter than the electron mean free path and longer than the angstrom-level atomic bond length, inducing the formation of minibands. To date mainly two types of electronic superlattices have been demonstrated: (1) vertically stacked layers with alternating composition, widely used for quantum cascade lasers and infrared photodetectors^{1,2}; (2) lateral two-dimensional (2D) Moiré superlattices composed of lattice-aligned graphene/hexagonal boron nitride (hBN) heterostructures,^{3–6} which are promising for plasmonic modulations and light-harvesting applications.^{7,8} However, both systems require lattice-matching conditions, which pose constraints on the choice of materials composition and the extent of device applications.

Self-assembly of solution processed nanoparticles is a low-cost method for nanostructure engineering, which can produce large-area close-packed superlattices having overall polycrystalline order and local crystalline domains.^{9–11} Despite the high structural quality, superlattice miniband effects have not been experimentally observed in these systems, largely due to the presence of defects on the (semiconducting) nanoparticle surfaces and the weak inter-particle electronic coupling.^{12–14} Here we demonstrate a new way to design a 2D superlattice device by integrating solution processed dielectric nanoparticles with 2D materials to form a heterostructure (Fig. 1a), which takes advantage of both the structural versatility of the nanoparticle assemblies and the high mobility of the 2D materials. We observe superlattice miniband conduction in a polycrystalline system where graphene

(Gr) is quasi-periodically deformed on top of SiO₂ nanospheres (NSs). We find that the size dispersion and imperfect ordering of the NSs induces broadening in the miniband density of states. While this effect is not ideal for applications where sharp states are needed (e.g., lasers and single-color LEDs), it can be beneficial for optoelectronic systems that require broadband modulation of the optical spectrum, such as optical modulators,¹⁵ photo-thermal conversion,^{16,17} infrared sensors,¹⁸ and optical communication.¹⁹ While currently we are using CVD grown graphene, this superlattice fabrication method is compatible with solution processed 2D materials.²⁰ Fully solution processed superlattices can enable low-cost large-area applications.

RESULTS AND DISCUSSION

Device fabrication and electronic transport

We use SiO₂ NSs for heterostructure fabrication because of their insulating nature, clean surface chemistry (terminated with hydroxyl groups and without organic capping molecules), and the ease of comparison with flat SiO₂ substrates (same surface chemistry with hydroxyl group termination). The NSs are packed in a polycrystalline structure where each single-crystalline domain consists of tens to hundreds of NSs; within each domain the NSs are hexagonal close packed (Fig. 1b, c). Our previous study shows that, after stacking graphene on top of these spheres, Gr bends and stretches around the apex of the NSs, giving rise to a quasi-periodically varying strain pattern.²¹ Within the experimentally accessible NS diameter range of 20–200 nm (spheres will have irregular shape and large size dispersity if diameter is less than 20 nm), we found that the overall strain in graphene is largest for the smallest sphere diameter.²¹ Therefore, here we choose the NSs with 20 nm diameter to induce a strain superlattice in Gr and

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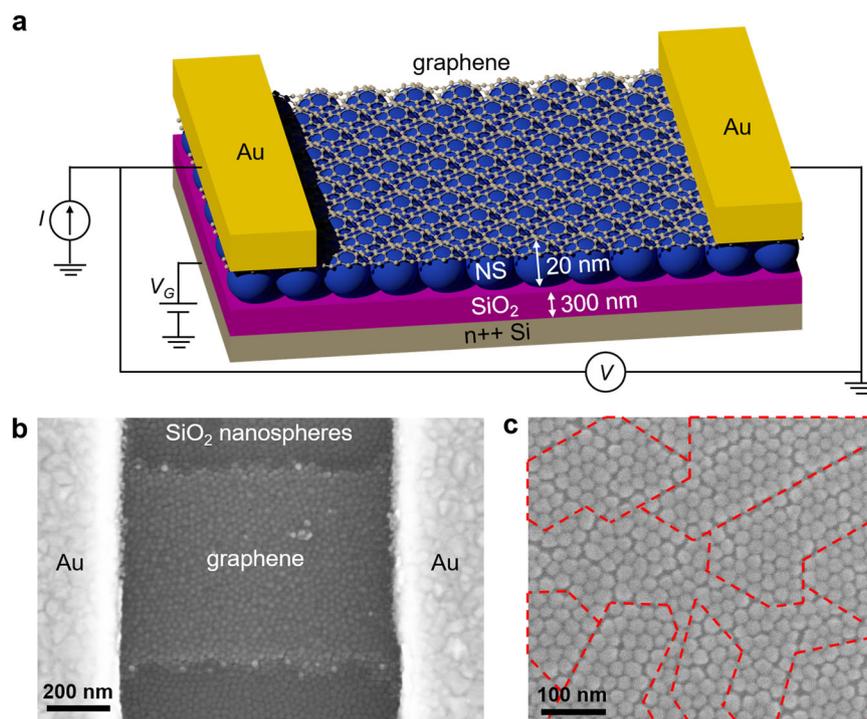


Fig. 1 Device schematics and images. **a** Schematic of the strain superlattice device structure. SiO₂ nanospheres (NSs) with 20 nm diameter are assembled on 300 nm SiO₂/n++ Si substrate. Graphene is stacked on top of the NSs and contacted by 1 nm Cr/110 nm Au. Channel length and width are between 0.6–2.4 μm in all the fabricated devices. **b** Scanning electron microscopy (SEM) image of one Gr–NS superlattice device, showing the Au contacts, SiO₂ nanospheres, and graphene on nanospheres. **c** High-resolution SEM images of a monolayer NS assembly, where each region enclosed by red dashed lines is a single-crystalline domain

study the electronic transport. This Gr–NS system shows periodic strain variations in graphene with a peak-to-peak magnitude in the scale of ~2%.²¹

We fabricated back-gated 2-terminal devices with Au contacts (Fig. 1a, b), and measured the electronic transport behavior of the Gr–NS systems; we also studied control samples consisting of graphene on flat SiO₂/Si substrate (see Methods for details). All the transport results shown here were obtained at 2 Kelvin. Figure 2a shows the conductance (G) as a function of gate voltage (V_G) for two control devices (Gr on flat SiO₂ substrate, labeled Gr1 and Gr2), which exhibit increasing conductance with gradually decreasing slope at both sides of the Dirac points (DPs). These are characteristic features of graphene-on-SiO₂ devices due to the coexistence of long and short-range scatterers.^{22–24} Gr on NS devices (labeled Gr-NS1, 2, 3), in contrast, show emergent conductance dip/kink features in the G vs. V_G curves (Fig. 2b). Remarkably, although the kink features occur at different gate voltages for separate devices, all of them are ~15 V away from their DPs. This same separation for different Gr–NS devices indicates that the conductance dips have the same origin. To remove the effect of the (doping induced) DP offsets and the device geometry on the transport characteristics, we plot the conductivity (σ) as a function of gate-tuned carrier density (n) for the same devices in Fig. 2c. Note that conductivity is defined as $\sigma = G \frac{L}{W}$, where G is the conductance, L is the channel length, and W is the channel width (Supplementary Section 1.1 shows the values of L and W and the method to convert gate voltage to n). Now it is evident that all three Gr–NS devices show dip features near $n = \pm 1 \times 10^{12} \text{ cm}^{-2}$ (corresponding to a V_G position of ~15 V away from the DP), while the amplitude of the dips varies among different devices and between the electron and hole sides. Note that all the Gr–NS devices show nearly the same minimum conductivity at DPs ($\sigma \cong 2 \frac{e^2}{h}$), indicating that all the devices have negligible amounts of random vacancy defects and cracks.

To further quantitatively compare the magnitude of the conductance kinks among different devices, we follow a well-developed protocol to normalize the conductance curves,²² which involves subtracting a series resistance (originating from contact resistance and short-range scatterers) from each curve to restore the linear background, and multiplying the curves by constant factors to normalize them to the same scale (Supplementary Section 1.2). As shown in Fig. 2d, after this normalization procedure, the control sample shows linear conductivity at both sides of the DP. The curves for all the Gr–NS devices perfectly overlap with that of the control sample at $|n| > 1 \times 10^{12} \text{ cm}^{-2}$, and show clear slope-changing features at the characteristic carrier density of about $\pm 1 \times 10^{12} \text{ cm}^{-2}$. The magnitude of the divergence from that of the control device is a measure of the amplitude of the conductance dips of the Gr–NS systems. Note that the electron and hole sides are processed separately for each curve, with different normalization factors, and therefore they do not necessarily align at the DP.

The position of the conductance dips matches with the commensurate filling of four electrons per superlattice unit cell (this number originates from the 4-fold spin and valley degeneracies in graphene). This can be seen by taking the lattice constant of the superlattice to be $\lambda \sim 21 \text{ nm}$ (~20 nm NS diameter and ~1 nm gap between adjacent NSs), and using the supercell area $A = \sqrt{3}\lambda^2/2 \approx 4 \times 10^{-12} \text{ cm}^2$. Then, one electron per supercell corresponds to a carrier density of $n_0 = 1/A = 2.5 \times 10^{11} \text{ cm}^{-2}$, and the dips occur at $n = \pm 4n_0 = \pm 1 \times 10^{12} \text{ cm}^{-2}$. The excellent match of the filling number with the theoretically expected value is strong evidence that the dip features are a consequence of superlattice effects, corresponding to superlattice Dirac points (SDPs). These SDPs occur at the mini-Brillouin-zone boundaries due to the superlattice modulation, where the small density of states leads to dips in conductance.^{4–6,25}

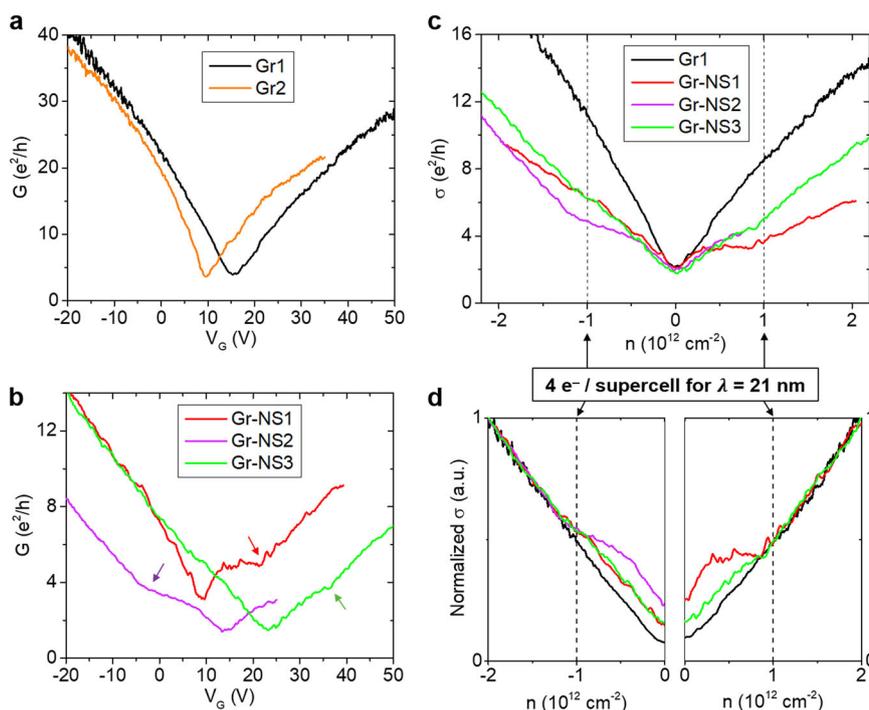


Fig. 2 Experimental superlattice transport. **a** Conductance (G) vs. gate voltage (V_G) curves for two control devices (Gr on flat SiO_2) Gr1 and Gr2. **b** G vs. V_G curves for three batches of Gr on 20 nm NS devices as labeled. **c** Conductivity (σ) vs. carrier density (n) for a control device (Gr1) and three Gr-NS superlattice devices. The conductivity of Gr1 is multiplied by a factor of 1/2 in order to fit to the same scale as other devices. **d** Normalized conductivity for the same devices shown in **c** (detailed normalization procedures discussed in Supplementary Section 1.2). Vertical dashed lines mark the positions of superlattice Dirac points (SDPs) in all the figures, corresponding to a carrier density of four electrons/holes per supercell. All the transport results shown here were obtained at $T = 2$ K

From the perspective of materials design, the widely studied graphene/hBN system allows a maximum superlattice period of ~ 14 nm, limited by lattice mismatch conditions of the constituent layers.^{4–6} As a result, the SDP position of Gr/hBN systems is at least $\sim 2.4 \times 10^{12} \text{ cm}^{-2}$. Our Gr-NS system offers a route to tune SDP positions in a larger range, including small carrier densities ($< 2 \times 10^{12} \text{ cm}^{-2}$) that are easily accessible via gate tuning. To further demonstrate this capability, we fabricated and measured a Gr-NS device where the NSs have a diameter of ~ 50 nm. Transport results reveal an intriguing conductance oscillation with a periodicity of $\sim 4.5 \times 10^{10} \text{ cm}^{-2}$, corresponding to one electron per supercell (Supplementary Fig. S2c, d), where the supercell now corresponds to the 50 nm NSs. Note that the same $1 e^-/\text{supercell}$ oscillation feature ($\sim 2.5 \times 10^{11} \text{ cm}^{-2}$ periodicity) is also present in the 20 nm system Gr-NS1, in addition to the SDPs at $4 e^-/\text{supercell}$ ($\sim 1 \times 10^{12} \text{ cm}^{-2}$) (Supplementary Fig. S2a, b). Overall, the $4 e^-/\text{supercell}$ feature occurs in all of the measured devices with 20 nm spheres, while the $1 e^-/\text{supercell}$ feature only occurs in some of the devices. Similar transport behavior has recently been observed in bilayer graphene and trilayer graphene-hBN superlattices, and explained as electron correlation effects.^{26,27} While the exact mechanism behind these transport features is still under study and is beyond the scope of this paper, the dip/oscillation features at commensurate filling for Gr-NS systems having two different NS sizes are strong evidence of superlattice effects.

To examine the effect of strain on the superlattice transport properties, it is desirable to deliberately modify the strain of a device while leaving other parameters unaltered, and observe the change in transport features. Previous work shows that temperature cycling can lead to compressive strain in an initially strain-free flake of Bi_2Se_3 contacted by electrodes.²⁸ Here we use the same approach to alter the strain properties of our system. After cooling down from 300 K to 2 K, and then warming up to 300 K again, we

find that, via Raman spectroscopy, the doping remains nearly the same while the spatially averaged tensile strain decreases by $\sim 20\%$ (Fig. 3a, Supplementary Section 1.5). The actual change of the nanoscale strain variation amplitude, or the RMS (root mean square) strain, can be much larger than the shift of average strain (Supplementary Section 1.5, Tables S2 and S3). Meanwhile, transport measurements of a Gr-NS device (Gr-NS2) reveal that the superlattice dip feature becomes much weaker after temperature cycling, compared to the same device before the thermal process (Fig. 3b, c). From the transport results, we also extract the mobility values (proportional to the slope of the curves for $n < -1 \times 10^{12} \text{ cm}^{-2}$) and find it to have only a minor change ($\sim 6\%$ decrease) after temperature cycling, revealing that the modifications of structural defects are small. Therefore, we conclude that strain modulation is likely the major factor contributing to superlattice transport features in the Gr-NS devices.

In Fig. 3c, we show how the amplitude of the conductance kinks at SDPs can be quantified by the slope changing angle in the normalized conductivity curves (θ_1 and θ_2 for Gr-NS2 before and after temperature cycling, respectively). We observe that $\theta_1 > \theta_2$, which quantitatively confirm the weakening of superlattice modulations. This conductance normalization and “kink angle” method can be generally used to quantify the amplitude of broad conductance dip features in polycrystalline or polydisperse superlattice systems.

In addition to the temperature cycling studies, to decisively prove the strain effect on superlattice transport, we prepared an extra control sample where 20 nm SiO_2 NSs are assembled on top of graphene on a flat SiO_2 substrate. Compared to the graphene-on-NS samples, this control sample is expected to have similar amounts of impurity, doping, and scattering at the graphene-NS interface, but strain will be absent since graphene lies on the flat substrate. Electronic transport results, shown in Supplementary

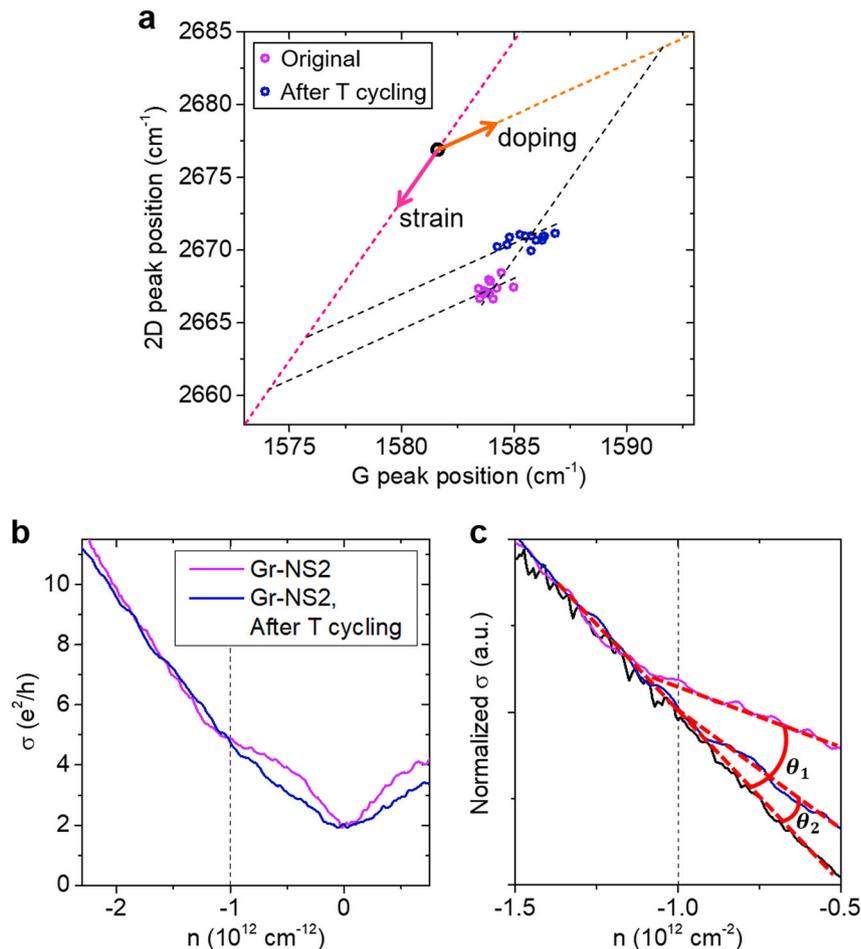


Fig. 3 Experimental strain manipulation and the effect on superlattice transport. **a** Correlation analysis of the measured Raman G and 2D peak positions, revealing a decrease of spatially averaged strain by $20\% \pm 4.9\%$ after temperature cycling. In contrast, the average doping value shows negligible change (an increase of $2.3\% \pm 8.8\%$). Each point represents a spectrum obtained at an optical pixel with a size of $\sim 0.5 \times 0.5 \mu\text{m}^2$ (details in Supplementary Section 1.5). **b** Conductivity vs carrier density for Gr-NS2, after the first cool down to 2 K (purple curve), and after warming up to 300 K then cooling down to 2 K again (dark blue curve). **c** Normalized conductivity for the same devices shown in **b**, and the control device Gr1 (black curve, same as that in the left panel of Fig. 2d). The curves are expanded to a carrier density range close to the SDP, and the kink angles of the Gr-NS2 device before and after temperature cycling are labeled as θ_1 and θ_2 , respectively

Fig. S3, reveals that a NS-on-graphene device exhibit no conductance dip feature. This result further proves that: (1) the conductance dip features of the Gr-NS devices are due to superlattice effects, instead of random scattering induced by the NSs; (2) strain modulation is the key factor contributing to the superlattice effects in the Gr-NS systems.

Quantum transport simulations

While our previous work has revealed periodic strain variations in the Gr-NS systems,²¹ and now we have experimentally observed the effect of strain on electronic transport in the superlattice (Fig. 3), it is still worth to theoretically examine all the possible factors that can contribute to superlattice transport. One possibility is doping modulation. It is known that random charged impurities are present on the SiO₂ surface, which induce p-type doping and charge fluctuations (or charge puddles) in the graphene layer on top.^{23,24,29–32} In our Gr-NS samples, the random charged impurities (with a concentration n_i) on the NS surfaces, together with the spatial variation of Gr to NS distance, determine the potential distribution of the graphene. From our experimental transport results, we estimate that $n_i \sim 7 \times 10^{11} \text{ cm}^{-2}$ (Supplementary Section 1.6), which agrees with previous reports.^{23,24,29–31} This corresponds to ~ 3 charged impurities per supercell on average,

given that the NS diameter is only 20 nm. Considering the random, discrete, and sparse distribution of these impurities, we expect the induced potential modulation in graphene to be mostly random and produce no superlattice effects. This is confirmed by our Coulomb potential and quantum transport simulations (Supplementary Section 2.5).

Another possible superlattice modulation factor is the gate-induced electrostatic potential variation in graphene resulting from its inhomogeneous dielectric environment. However, due to the small height variations of graphene (~ 2 nm, determined from atomic force microscopy) and the small size of spheres (20 nm) compared to the thickness of the flat SiO₂ dielectric layer (300 nm), we expect the gate-tuned carrier density in graphene to be nearly homogeneous. Our electrostatic simulation confirms that, within the experimental range of gate voltage, the gate-induced variation in electrostatic potential is smaller than the random potential fluctuations in Gr caused by the charged impurities on the SiO₂ surface (Supplementary Section 1.7). As a result, the electrostatic contribution to superlattice transport should be negligible. This is in agreement with our experimental result shown in Fig. 2b, where we find a strong SDP feature for Gr-NS2 on the hole side occurring near zero V_G , revealing that superlattice transport can occur without any electrostatic modulation.

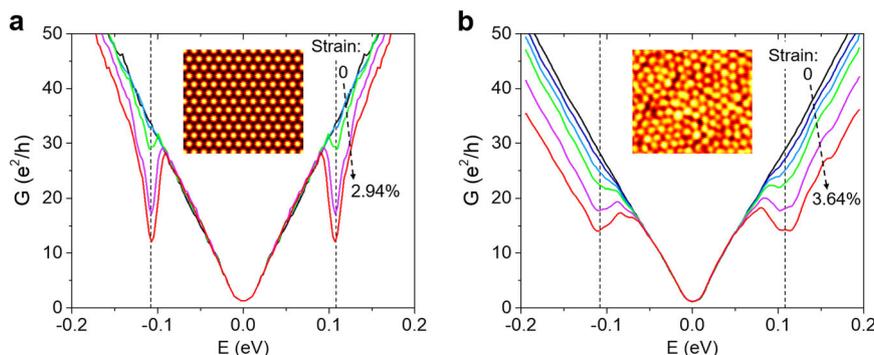


Fig. 4 Quantum transport simulations. **a** Simulated conductance (G) vs. energy (E) curves for graphene on single crystalline NSs (packing structure shown in the inset), with different RMS strain values of 0, 0.28%, 1.11%, 2.02%, 2.94% from top to bottom (black to red) (details shown in Supplementary Section 2.3). **b** Simulated G vs. E curves for graphene on polycrystalline NSs. The simulated NS packing structure, as shown in the inset, is adopted from our experimental image. From top to bottom (black to red), the curves correspond to RMS strain values of 0, 0.99%, 1.42%, 1.86%, 2.75%, 3.64% (details shown in Supplementary Section 2.4). Vertical dashed lines mark the expected SDP position at $E_{\text{SDP}} = \pm \frac{h v_F}{\sqrt{3} a} = \pm 0.11$ eV, where h is the Planck constant and $v_F = 1 \times 10^6$ m/s is the Fermi velocity of graphene³

To further quantify the effect of strain variations on carrier transport, we perform tight-binding transport simulations incorporating the experimentally relevant NS size and distribution and Gr strain variation parameters (details in Supplementary Sections 2.1 and 2.2). We use the following formula to relate the bond length to the hopping parameter (t) in the tight binding Hamiltonian:

$$t + \delta t = t \exp(-\beta(l/a - 1)), \quad (1)$$

where a and l are the bond length of the unstrained and strained graphene, respectively, and $\beta = 3.37$ is a constant parameter.³³ We chose a range of strain magnitude, and simulate the conductance of the Gr-NS system with both single-crystalline and polycrystalline packing structures (Fig. 4a, b). Note that we directly imported the experimentally imaged NS packing profile for simulation of the polycrystalline system, shown in the inset of Fig. 4b (see also Supplementary Fig. S11). The unstrained graphene (Gr on flat SiO₂ substrate) system shows the standard transport features of graphene with no superlattice conductance dips. When strain is added, SDPs appear at the expected energy levels, and become more evident as strain is increased, for both the single-crystalline and polycrystalline systems. The main difference between these two systems is that the polycrystalline devices exhibit broader conductance dips due to the structural disorder. The simulation results on the polycrystalline system are in good agreement with the experimental data in Fig. 2b–d, and imply that the variations in the magnitude of the dip features in different experimental Gr-NS devices can be attributed to differences in strain amplitudes. For example, comparing Fig. 2c, d with Fig. 4b, we can roughly estimate that the RMS strain values of Gr-NS2 and Gr-NS3 are ~2% and ~1% (by comparing the kink angles), respectively. Other factors, such as fluctuations in charge doping, mobility, and NS ordering are either negligible or do not correlate with the change of dip features (Supplementary Section 1.8). The strain variation among different samples is likely due to the device fabrication and cooling down processes.

In summary, we have created a large-area applicable superlattice device by stacking graphene on solution processed assemblies of SiO₂ NSs. Electronic transport measurements reveal strain-tunable conductance dips due to superlattice miniband effects. Key evidences for superlattice transport in the Gr-NS devices are: (1) conductance dips occur at $4e^-$ per supercell for all the Gr-NS devices, which diminish when strain is reduced; (2) control devices of flat Gr and NS-on-flat Gr do not show conductance dips; (3) transport simulations of Gr-NS systems incorporating the actual polycrystalline NS packing structure

reveal strain-dependent conductance dips, similar to the experimental results.

We expect that our hybrid heterostructure, combining solution-processed, self-assembled nanoparticle superlattices, and atomically thin 2D materials (with superior flexibility compared to bulk^{34–37}), will be a powerful framework to design a variety of “artificial solids” that enable band structure engineering via real space patterning. These superlattice devices are cost-effective to manufacture, and are promising for large-area, broadband optoelectronic applications such as optical modulators, infrared sensors, and photothermal converters.^{15–19}

MATERIALS AND METHODS

Sample preparation

SiO₂ NSs with 20 nm diameter were purchased from nanoComposix, product number S1SN20-10M. The surfaces of these NSs are clean with only hydroxyl groups covering them (no organic capping ligands). The NSs were dispersed in water with a concentration of 5 mg/mL. 300 nm SiO₂/n++ Si substrates were cleaned by acetone, IPA, and O₂ plasma, followed by spin-coating of the NSs. The sample was then baked on hotplate at 170 °C for 20 min to remove the residual water. The NSs were attached to the SiO₂/Si surface with sub-monolayer coverage on the whole substrate, and closely packed monolayer domains in the scale of microns to tens of microns were observed. CVD graphene (purchased from ACS Material) was transferred to the NS substrate using the standard wet-transfer techniques,³⁸ followed by critical point drying to avoid ripping of graphene. We observed both regions of graphene on top of the NS monolayers and regions of Gr on the flat SiO₂ substrate on each sample.

Device fabrication and measurements

Confocal Raman spectroscopy was performed to identify defect-free areas of graphene for device fabrication. E-beam lithography was performed to define 2-terminal electrodes for both the Gr-NS regions and the flat Gr regions, followed by thermal evaporation of 1 nm Cr/110 nm Au. The gap between each pair of leads is between 0.6–2.4 μm, and these leads provide structural support for the graphene in the channel region during the following fabrication steps. This is important for the Gr-NS systems where free-standing regions of graphene (between the neighboring NSs) are fragile. For the same reasons, previous high-quality transport measurements of free-standing graphene were performed on 2-terminal devices instead of multi-terminal Hall bar devices.³⁹ Subsequently, another e-beam lithography step was performed to define etch patterns, and O₂ plasma was used to etch graphene into rectangular areas between the 2-terminal leads. After each lithography and lift-off step, the samples were dried in a critical point dryer to avoid structural degradation. The completed devices were wire-bonded and measured in a physical property measurement system under vacuum conditions. An AC current source (10 nA, 17 Hz) was applied to the Au source/drain leads to measure the resistance using a

lock-in amplifier, while gate voltage was applied to the Si substrate to tune the carrier density.

Raman spectroscopy

Confocal Raman spectroscopy was performed using a Nanophoton Raman 11 system at room temperature, with an excitation wavelength of 532 nm. 100× objective was used and the laser power was between 0.5–1 mW. All the measured spectra were calibrated using the emission lines of a neon lamp.

Transport simulations

A tight-binding model was used to construct the model Hamiltonian for graphene and observables were computed using non-equilibrium Green's function formalism. The form of the Hamiltonian and simulation details are available in Supplementary Section 2.

DATA AVAILABILITY

The data used in this study are available upon reasonable request from the corresponding author Y.Z. (yjz@illinois.edu).

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AUTHOR CONTRIBUTIONS

Y.Z. conceived the experiment. Y.Z. designed and fabricated devices, and carried out transport measurements. Y.K. and M.J.G. performed the transport simulations. Y.Z., Y.K., M.J.G., and N.M. analyzed the data and wrote the manuscript.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (<https://doi.org/10.1038/s41699-018-0076-0>).

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